

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

---

BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

---

Ex parte MARK I. GARDNER, ROBERT DAWSON,  
H. JIM FULFORD JR., FREDERICK N. HAUSE,  
MARK W. MICHAEL, BRADLEY T. MOORE and DERICK J. WRISTERS

---

Appeal No. 2000-0732  
Application No. 08/741,799

---

ON BRIEF

---

Before KRASS, FLEMING, and DIXON, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1-16, 19-29 and 44-53, all of the remaining claims.

The invention is directed to a method for retarding upward diffusion of a dopant within a semiconductor body. More particularly, a barrier layer of material is formed by implanting the material through the top portion of the semiconductor body so as to form the barrier layer below the top surface of the semiconductor body and at a depth greater than the depth of a source/drain region within the semiconductor body.

Representative independent claim 1 is reproduced as follows:

1. In a semiconductor process, a method of retarding upward diffusion of a dopant within a semiconductor body, said method comprising the steps of:

providing a semiconductor body having a top surface and a heavily-doped layer beneath and separated from the top surface, said heavily-doped layer including a first dopant;

forming a transistor gate electrode over the semiconductor body;

forming a transistor source/drain region within the semiconductor body; and

implanting a material through a top portion of the semiconductor body to form a barrier layer of said material beneath and separated from the top surface and at a greater depth than the source/drain region, for retarding the upward diffusion of said first dopant.

Appeal No. 2000-0732  
Application No. 08/741,799

The examiner relies on the following references:

Kuroi	5,578,507	Nov. 26, 1996 (filed May 11, 1995)
Kato	5,654,209	Aug. 05, 1997
Aronowitz et al. (Aronowitz)	5,654,210	Aug. 05, 1997 (filed May 4, 1995) (filed Oct. 19, 1994)

Wolf, "Silicon Processing For The VLSI ERA" Lattice Press,  
vol. 3, (1995), pp. 554-555.

Claims 1-4, 6, 8, 10, 11 and 14-16 stand rejected under  
35 U.S.C. 102(e) as anticipated by Kato.

Claims 5, 7, 9, 12, 13, 19-29 and 44-53 stand rejected  
under 35 U.S.C. 103. As evidence of obviousness, the examiner  
cites Kato and Wolf with regard to claims 5 and 7, Kato and  
Aronowitz with regard to claim 12, Kato and Kuroi with regard  
to claims 9, 13, 19-23, 26-29, 44-46 and 50-53, and Kato,  
Kuroi and Wolf with regard to claims 24, 25 and 47-49.

Reference is made to the briefs and answer for the  
respective positions of appellants and the examiner.

#### OPINION

At the outset, we note that, in accordance with

appellants' grouping of the claims at page 4 of the principal brief, all the claims will stand or fall together. Accordingly, we will concentrate our comments on independent claim 1.

Claim 1 stands rejected as being anticipated by Kato. As we understand it, it is the examiner's position that Kato's semiconductor device is considered to have a semiconductor body (comprising substrate 10 and epitaxial layers 13 in combination), wherein the top surface of the semiconductor body is the top surface of the epitaxial layers 13. Embedded layer 11 is then considered the claimed "heavily-doped layer beneath and separated from the top surface" and including a first dopant since the N<sup>+</sup> material of embedded layer 11 is more heavily doped than the N material of the epitaxial layers 13. The examiner points to gate 22 in Figure 2(f) and to source/drain regions 27 in Figure 2(g) of Kato and indicates that the gate is formed over the semiconductor body and the source/drain regions are formed within the semiconductor body.

Up to this point, the examiner's analysis and application of Kato to the instant claimed subject matter appears reasonable.

Claim 1 then goes on to recite: "implanting a material through a top portion of the semiconductor body to form a barrier layer of said material beneath and separated from the top surface and at a greater depth than the source/drain region, for retarding the upward diffusion of said first dopant."

The examiner refers to Kato's embedded layer 11 as the implanted material. While we agree that layer 11 does appear to form a barrier layer and is separated from the top surface of epitaxial layers 13 at a greater depth than the source/drain regions 27 in Kato, it is not clear to us that layer 11 in Kato is achieved by "implanting...through a top portion of the semiconductor body," as required by the claim.

If the instant claims were directed to a structure, the process by which that structure was made would be irrelevant. However, the instant claims are directed to methods having a particular order of steps. Thus, even though Kato shows embedded layer 11, it is important to ascertain how that layer was formed. From Kato's disclosure, at column 5, line 66-column 6, line 5, it would appear that layer region 11 is embedded in the main surface of the substrate 10 *prior* to the

time the epitaxial layer 13 is grown. Since, in the examiner's analysis, the top surface of epitaxial layer 13 is the top surface of the semiconductor body, it cannot be said that this embedded layer 11 is implanted "through a top portion of the semiconductor body," as claimed.

Now, at column 6, lines 23-24, of Kato, it is recited that "[t]he N+ embedded layer 11 can also be formed by ion implantation at high energy..." and this might imply that the layer is implanted *through* another layer (e.g., epitaxial layer 12) into substrate 10. However, it may just as well mean that, just as before, layer 11 is formed in substrate 10 before the epitaxial layer 13 is grown but that layer 11 is formed by implanting, at high energy, into the surface of substrate 10. This latter choice is the more likely one since Kato does not indicate any deviance from the prior disclosure of growing the epitaxial layer 13 after the formation of layer 11 within substrate 10. In any event, if Kato is ambiguous on this point, to find that layer 11 is implanted through the epitaxial layer, i.e., through a top portion of the semiconductor body, as claimed, we would need to resort to speculation. An ambiguous reference will not support a

Appeal No. 2000-0732  
Application No. 08/741,799

section 102 rejection. In re Hughes, 345 F.2d 184, 145 USPQ 467 (CCPA 1965).

We also note appellants' argument regarding the claimed recitation of the implantation "for retarding the upward diffusion of said first dopant." We agree with appellants that Kato teaches that a "redistribution" in the embedded layer 11 can be prevented [see column 6, lines 10-11] and says nothing about retarding "upward diffusion" of the dopant. It is the examiner's position that the effect of unwanted redistribution would "include upward diffusion" [see page 6 of the answer] but the examiner points to nothing which would support this position. Now, it may be that if all the claimed method steps were taught by Kato, an inherency argument would lie since a structure achieved by employing the same process as that claimed would appear to "inherently" exhibit the same properties, viz., retarding the upward diffusion of the first dopant. In any event, no inherency argument has been made by the examiner and it is our view that Kato does not disclose the same method set forth in instant claim 1.

Accordingly, we will not sustain the rejection of claim 1, and of claims 2-4, 6, 8, 10, 11 and 14-16 dependent

thereon, under 35 U.S.C. 102(e) over Kato. Since neither Wolf, Kuroi nor Aronowitz provides for the deficiencies of Kato, noted supra, and we find no reason to hold the implantation of layer 11 in Kato through the epitaxial layer 13 to have been obvious, we also will not sustain the rejection of claims 5, 7, 9, 12 and 13 under 35 U.S.C. 103.

Independent claims 19 and 44 are similar to claim 1 except that they specifically recite the heavily-doped layer as being a P+ layer including boron and that the material implanted is nitrogen. Additionally, claim 44 requires two implantations and a final annealing step. However, neither independent claim 19 nor independent claim 44 includes the claim 1 limitation of implanting "through a top portion of the semiconductor body."

Accordingly, appellants' arguments directed to implanting "through a top portion of the semiconductor body" has no relevance to independent claims 19 and 44.

Further, appellants offer no argument regarding the P+ nature of the dopant, that the layer includes boron or that

the material implanted is nitrogen. Accordingly, we accept the examiner's rationale with regard to these claim limitations.

At page 6 of the principal brief, appellants argue that Kato and the claimed invention are distinguished by "comparing Kato's depth profiles of Figures 9 and 11 (both of which indicate surface deposition of the element of high electronegativity) with the appellants' disclosed barrier layer depth profiles in, for example, Figure 7." We do not find this argument to be persuasive since appellants never state what, exactly, that distinction is after inviting us to compare Figures 9 and 11 of Kato with Figure 7 of the instant application.

Thus, we are left with the argument that Kato does not teach or suggest a method that retards the upward diffusion of dopants. The examiner contends that Kato's reduction of redistribution encompasses upward diffusion but, as we said supra, the examiner has offered no evidence to support this allegation. Again, we will not conjecture as to whether an "inherency" argument could have been made in this regard since the examiner has not made it.

Appeal No. 2000-0732  
Application No. 08/741,799

Accordingly, we find that the examiner has not established a prima facie case of obviousness, within the meaning of 35 U.S.C. 103, and we will not sustain the rejection of claims 19-29 and 44-53 under 35 U.S.C. 103.

Since we have not sustained any of the rejections of the claims, the examiner's decision is reversed.

REVERSED

ERROL A. KRASS	)	
Administrative Patent Judge	)	
	)	
	)	
	)	
	)	
MICHAEL R. FLEMING	)	BOARD OF PATENT
Administrative Patent Judge	)	APPEALS AND
	)	INTERFERENCES
	)	
	)	
	)	
JOSEPH L. DIXON	)	
Administrative Patent Judge	)	

Appeal No. 2000-0732  
Application No. 08/741,799

EK/RWK

SKJERVEN MORRILL MACPHERSON LLP  
25 METRO DRIVE  
SUITE 700  
SAN JOSE, CA 95110